AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

On page 3, paragraph [0007]:

[0007] FIG. 2 is a block diagram further illustrating a processor of FIG. ~~2~~1, in accordance with the further embodiment of the invention.

On page 6, paragraph [0020]:

[0020] Chipset 180 is comprised of a memory controller, or memory controller hub (MCH) 120, as well as an input/output (I/O) controller or I/O controller hub (ICH) 130. Memory controller 120 is coupled to main memory 140 and one or more graphics devices or graphics controller 160. In one embodiment, main memory ~~110~~-140 is volatile memory, including but not limited to, random access memory (RAM), dynamic RAM (DRAM), synchronous DRAM (SDRAM), double data rate (DDR) SDRAM, rambus data RAM (RDRAM) or the like. In addition, hard disk drive devices (HDD) 150 and I/O devices 170 (170–1, . . ., 170-N) are coupled to I/O controller 130. Adaptive prefetch logic 200 is further illustrated with reference to FIG. 2.

On page 6, paragraph [0021]:

[0021] FIG. 2 further illustrates CPU 110 of FIG. 1 to further describe adaptive prefetch logic 200. CPU 110 is comprised of processor core 112, which may include, for example, copy-back cache (not shown), as well as level one cache (L1) 114 for high speed temporary storage of data. In addition, processor or CPU 110 may include level two cache (L2) 120 as well as copy-back cache 122. As illustrated, L2 cache 120 is off chip memory coupled to backside bus unit 116 via, for example, backside bus 118. CPU 110 includes external bus unit 104 for interfacing with FSB 102 (FIG. 1) including in-order queue (IOQ)

130, as described below. However, in contrast to conventional CPUs, CPU 110 includes adaptive prefetch logic 200.

On page 10, paragraph [0031], please insert Equation (1):

$$\mu = \left(\sum n \right) / (t) \tag{1}$$

On page 10, paragraph [0032], please insert Equation (2):

$$\Lambda = \left(\sum n \right) / (\#R) \tag{2}$$